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THEORETICAL AND EXPERIMENTAL RESEARCH TO ASSIST IN PREPARATION AND DESIGN OF A HIGH FREQUENCY SILICON CARBIDE ACTIVE DEVICE

H. C. Chang, Principal Investigator

SCIENTIFIC REPORT NO. 1 and 2

Contract AF 19(604)-8499

January - 1962

Project 4608

Task 460804

Prepared

for

ELECTRONICS RESEARCH DIRECTORATE
AIR FORCE CAMBRIDGE RESEARCH LABORATORIES
OFFICE OF AEROSPACE RESEARCH
UNITED STATES AIR FORCE
BEDFORD, MASSACHUSETTS

WESTINGHOUSE RESEARCH LABORATORIES
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10 High Street
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ABSTRACT

The large band gap of silicon carbide makes it an interesting material for use in semiconductor devices which are operable at ambient temperatures in excess of 500°C. It has been shown that silicon carbide has a higher tolerance to radiation damage than silicon. The objective of the present program is a theoretical and experimental investigation of a high frequency silicon carbide transistor operable at 500°C, prepared by vapor-phase epitaxial growth techniques. The main advantage of the epitaxial growth method is the precise control obtainable over the junction structure.

An apparatus for investigating epitaxial growth by the thermal reduction of silicon and carbon compounds has been constructed. Preliminary results indicate growth has taken place although this growth shows structural defects. Junctions formed by this technique have shown rectifying properties. A diffusion process is being used as a supplementary method to prepare the junctions necessary for the high frequency transistor. Diffused junction crystals have been prepared for evaluation.

Perfection of device techniques are being pursued. Improved etching and junction delineation methods are described. Experimental designs for the transistors are discussed.

INTRODUCTION

The objective of this work is to study, develop, and apply techniques necessary to make active silicon carbide devices capable of oscillating and/or amplifying at a frequency of at least 1 Mc/s at a temperature of 500°C. To achieve this it is necessary to have the following:

1. Methods for preparing pure single crystals of silicon carbide.
2. Methods, such as epitaxial growth and diffusion, for producing rectifying junctions in silicon carbide.
3. Methods, such as chemical and electrochemical etching, for shaping silicon carbide into the desired form.
4. Methods such as alloying for making ohmic and rectifying contacts to silicon carbide.

Previous work on the fabrication of silicon carbide transistors has been reported[1,2]. The fabrication was achieved on an experimental model silicon carbide transistor which exhibited power gain up to 500°C. These transistors were made using high purity n-type alpha silicon carbide for the channel material and aluminum-diffused junctions for the gates. However, the latter diffusion is difficult to control since it requires relatively deep diffusion into both faces of a silicon carbide crystal, leaving a thin region, 5 microns thick, in the middle of the crystal to act as the channel. Therefore in the present work, the use of epitaxially grown silicon carbide for the fabrication of silicon transistor is under investigation.

The potential advantages of the epitaxial growth of silicon carbide are that it is possible to grow high-purity thin layers onto low purity silicon carbide substrates. It should be possible either to grow further layers or to diffuse into the first epitaxial layer in order to produce structures similar to epitaxial P*PIN silicon and germanium transistors. It is known that epitaxial silicon transistors[3] have lower switching times and lower saturation voltages when compared to conventional pnp or npn silicon and germanium transistors.

Also it is possible to use a high resistivity epitaxial layer, grown onto a low resistivity but opposite conducitivity type substrate, as the channel region for a unipolar transistor.

In the work on the epitaxial growth of silicon carbide, the layer is being grown by the hydrogen reduction at 1600°C to 1900°C of silicon tetrachloride and carbon tetrachloride. This method was chosen instead of using the previously tried technique of transport[2] by sublimation since the latter requires comparatively high growth temperature and is inconvenient for the control of doping and uniform growth. Also owing to high temperature required, diffusion of any dopants present produces a graded instead of an abrupt junction between the substrate and the epitaxial layer.

In support of the work on the epitaxial growth of silicon carbide some investigations have been carried out on the epitaxial growth of gallium arsenide by hydrogen reduction of trihalides of gallium and arsenic. Gallium arsenide was chosen for these investigations instead of the better known

silicon and germanium since like silicon carbide it is a binary semiconductor compound. The chemical reaction kinetics of the epitaxial growth of gallium arsenide were expected to be similar to those found for silicon carbide except that the growth of gallium arsenide should occur at much lower temperatures, below 1000°C, which would facilitate the study of the chemical reactions occurring.

However, it has been found that although arsenic trihalides are reduced to arsenic, gallium trihalides are not reduced to gallium below 1000°C. and therefore gallium arsenide cannot be obtained by this process. Thus this work has not produced the expected result and therefore is not described in this report.

2. EPITAXIAL GROWTH OF SILICON CARBIDE

2.1 THEORETICAL DISCUSSION

At present the epitaxial growth of silicon carbide is being investigated in this laboratory. The method that is being employed in this study involves the high temperature reaction of a gaseous mixture of silicon tetrachloride, carbon tetrachloride and hydrogen on a silicon carbide single crystal substrate.

The principal reaction variables in epitaxial growth are the temperature of the substrate, the chemical composition and concentrations of the gaseous reactants. In order to determine the optimum conditions for these variables the results of previous experiments on vapor growth of silicon carbide crystals has been reviewed. The vapor-growth process should be essentially the same as epitaxial growth except for the initial nucleation in the former. The vapor-growth work has given indications that there is a lower and upper temperature limit for growing large single crystals of silicon carbide. For example Straughan & Mayer [4] have reported that below 1500°C the vapor growth method using the reactants described above, generally gave only polycrystalline silicon carbide and free carbon and silicon. This may be explained by assuming that at this temperature the mobility of the silicon and carbon atoms are not large enough for these atoms to migrate to the lattice sites involved in single crystal growth. Therefore nucleation of the atoms to form silicon and carbon or polycrystalline silicon carbide may result. As for the upper temperature limit on vapor growth of silicon carbide Ellis [5] and others [6] have observed that at temperatures above 2000°C the silicon carbide crystal will decompose at an appreciable rate to carbon and silicon containing vapor species.

The cause of this decomposition can best be understood by an examination of the work of Drowart et al (7) who studied the high temperature thermodynamic properties of silicon carbide, with the use of a specially modified mass spectrometer. As shown in the table given below, these authors have found that at temperatures in the vicinity of 2000°C, the decomposition pressure of silicon carbide becomes appreciable.

PARTIAL PRESSURES OF THE VARIOUS SPECIES OVER SiC° IN ATMOSPHERES (7)

T °K	Si	SiC	SiC_2	Si_2C
2149	2.1×10^{-5}	2.2×10^{-9}	1.9×10^{-6}	1.4×10^{-6}
2168	2.7×10^{-5}		2.5×10^{-6}	1.9×10^{-6}
2181	3.3×10^{-5}	2.2×10^{-9}	4.2×10^{-6}	2.6×10^{-6}
2196	4.1×10^{-5}		4.4×10^{-6}	3.9×10^{-6}
2230	6.5×10^{-5}		6.5×10^{-6}	5.1×10^{-6}
2247	8.3×10^{-5}	6.3×10^{-9}	1.1×10^{-5}	8.1×10^{-6}
2316	2.0×10^{-4}	1.9×10^{-8}	3.1×10^{-5}	2.2×10^{-5}

The data in the above table also suggests a possible mechanism for the formation of silicon carbide. As indicated there silicon carbide gas is found above silicon carbide in very low concentrations, the major vapor species above silicon carbide being silicon gas. This would suggest that silicon carbide gas probably plays a minor role in the formation or decomposition of silicon carbide. A possible mechanism for the formation or decomposition of silicon carbide is that of silicon and carbon atoms being

formed at or near the hot crystal surface. After these atoms strike the crystal surface they have a certain probability to migrate to the growing lattice sites. If these atoms are not stabilized by being incorporated into the lattice the silicon and to a lesser extent the carbon atoms may be removed by simple evaporation or by reaction with the ambient gases such as H_2 or HCl.

The important point to emphasize here is that a mechanism of silicon carbide formation to be useful must be able to predict how crystal growth is affected by a change in the growth variables. If these predictions were correct, they would then serve to prove the existence of such a mechanism. There are other mechanisms such as the reaction of the gases SiC_2 and Si_2C on the crystal surface which might explain the experimental results if a series of complex steps were theorized. Hypothesizing such a complex mechanism does not however add to the ability to predict the consequences of changes in experimental conditions. Therefore the relatively simple mechanism described above should serve as a useful guide.

This mechanism may also explain the observation that toluene appears to give better results in silicon carbide vapor growth than the use of other carbon compounds such as methane or benzene. The explanation for this may be that the carbon atoms must be formed at a rate similar to the rate of the formation of the silicon atoms, otherwise the carbon and silicon atoms nucleate, independently. If this conclusion is correct then the ratio of $SiCl_4$ to Toluene or CCl_4 must be carefully adjusted.

2.2 EXPERIMENTAL

A diagram of the reactor being used in the epitaxial growth of silicon carbide is shown in Fig. 2.1. The pure hydrogen (Matheson Research grade) is passed through a purification train consisting of a Deoxo unit for catalytic oxygen removal, a chemical dessicant, anhydrous calcium sulphate and a cold trap filled with Linde 5A molecular sieves. The ultra pure hydrogen is then passed into a manifold connecting in parallel three Matheson flow meters. The latter have been selected to give as wide as possible variation in controlled gas flow in order to study a wide range of molar ratios of hydrogen to silicon tetrachloride and hydrogen to carbon tetrachloride. The argon inlet line is used initially to remove air from the system prior to the passage of hydrogen.

Two of the flowmeters are connected to two saturator flasks which are maintained at a constant temperature of 0°C by immersion in ice-water bath. The saturator flasks contain pure silicon tetrachloride and carbon tetrachloride. Hydrogen gas when passed over these liquids is saturated with vapor of the liquid. The vapor pressures at 0°C of silicon tetrachloride and carbon tetrachloride are 76.0 mm and 33 mm, respectively. Therefore by the partial pressure l a w the mole ratios at 0°C for hydrogen to silicon tetrachloride and hydrogen to carbon tetrachloride are 10 to 1 and 23 to 1 respectively.

The hydrogen passed through the saturator is then mixed by a mixing chamber with the "by-pass" hydrogen from the third flow meter. The combined gas stream is then fed into the reactor.

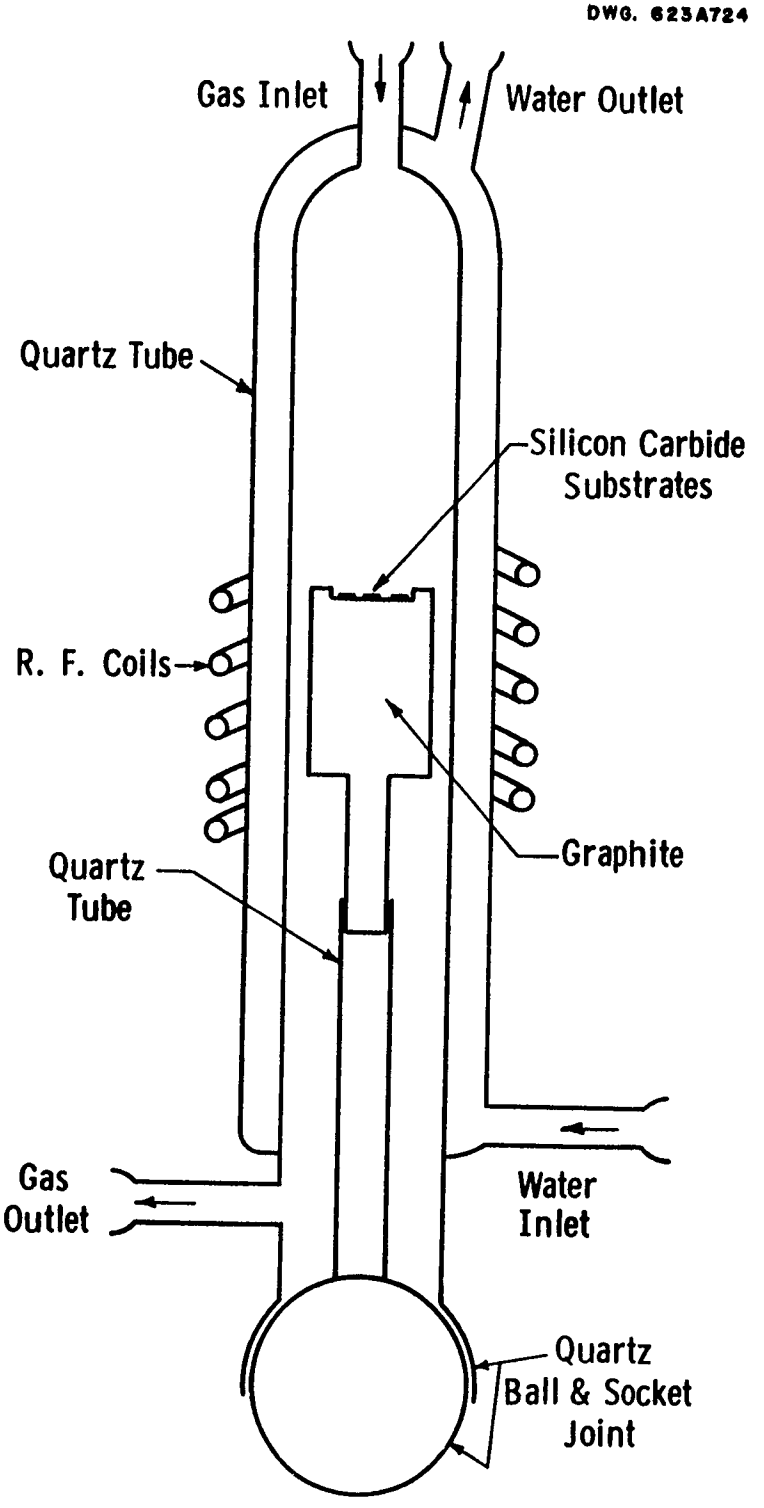


Fig. 2.1—Epitaxial growth reactor

The reactor is a water cooled quartz tube which is held vertically and inside of which is a cylindrical graphite block supported in a quartz holder. The graphite block is machined from United carbon UT6 or UF45 grade graphite. The block is heated by means of an external RF coil which is powered by a 10 kilowatt, 450 kilocycle, R.F. Generator. The temperature of the top surface of the graphite block and the temperatures of silicon carbide substrates placed on the top surface are measured by a optical pyrometer.

The hexagonal silicon carbide substrate was cleaned successively in methyl alcohol, hydrofluoric acid and distilled water. This treatment should remove grease and surface silicon oxides. The substrate was dried under an infrared lamp while protected from atmospheric dust particles. When dried the substrate was transferred to the top surface of the graphite heater using stainless steel tweezers. The substrate was touched by the tweezers only on its edges to avoid contamination of the flat surface which was to be grown upon.

The graphite heater was inserted into the quartz reactor tube and aligned with respect to the external R.F. Coil. The air inside the reactor tube was removed by passing through argon. Hydrogen was then admitted from the "by-pass" flowmeter and the graphite heated to the desired temperature, up to 1900°C. The gas flow through the by-pass and the saturator were adjusted to obtain the following ranges of conditions: total hydrogen 1 to 10^{-2} gram moles/minute, silicon-tetrachloride 0.7 to 2 x 10^{-4} gram moles/minute, and carbon tetrachloride 0.4 to 1 x 10^{-4} gram moles/minute. Normally the growth run was continued for a period of

at least sixty minutes. After the required time for growth the graphite was cooled rapidly to room temperature in a stream of hydrogen from the by-pass. The hydrogen was purged from the reactor tube using argon and the graphite heater was taken out.

The sample was removed from the graphite heater and was examined under reflected light using a Leiz microscope. Photomicrographs of typical surfaces are shown in Figures 2.2, 2.3 and 2.4 for runs 27, 28 and 32 respectively.

It may be seen from these photomicrographs that the surfaces have shown structural defects, in particular triangular growth. The presence of these triangles indicates that there are stacking faults of the atomic layers which are occurring during growth.[8] The cause of these defects is not known with certainty though it does not seem to be due to temperature since there is no marked change in the number of faults from 1550°C to 1700°C.

The thickness of the grown layer was obtained by bevelling the sample at an angle of 5 degrees using 320 grit boron carbide and 1 micron diamond paste for grinding and polishing, respectively. A photomicrograph of a typical bevelled sample, which shows the grown layer on the original substrate, is seen in Figure 2.5. Layers of silicon carbide have been grown from 12 to 70 microns thick. The growth rate above 1600°C is about 1 micron per minute.

Two samples with a 70 micron thick grown layer have been examined by a back reflection x-ray technique. The x-ray photographs obtained show patterns characteristic of hexagonal silicon carbide. However, since the influence of the substrate on the x-ray photographs is not known it cannot be

Fig. 2.2 Run 27 [x 200]

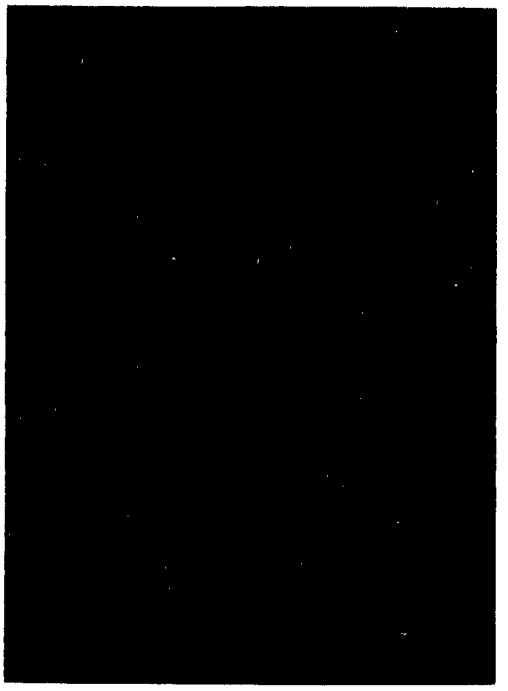


Fig. 2.3 Run 32 [x 100]

Typical Surfaces of SiC Grown Layer

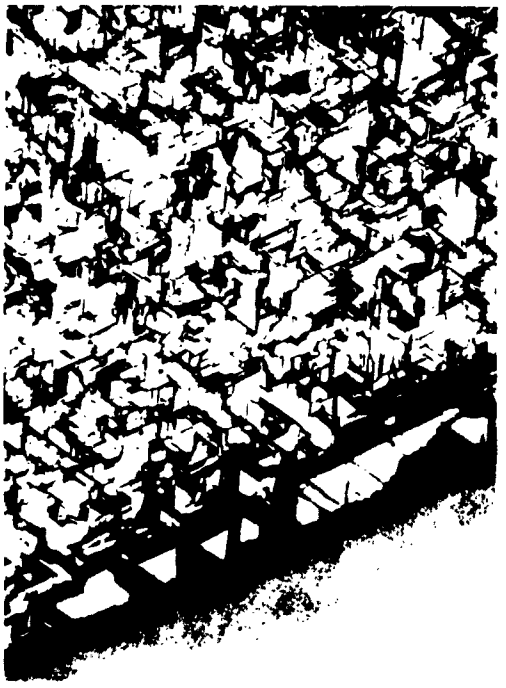


Fig. 2.4 Run 28 [x 100]

Typical Surface of SiC Grown Layer

Fig. 2.5 Run 24 [x 50]

Grown Layer Thickness as Delineated by 5° bevel method

definitely concluded that the layers are of hexagonal silicon carbide. Further work is being carried out on this problem.

During all growth runs small yellow crystals have grown on the graphite heater. These crystals have been identified as cubic silicon carbide by x-ray powder analysis.

2.3 DISCUSSION

At present the cause of the structural faults seen on the surface of the grown layer is uncertain. However some reasons for these faults are postulated here and these reasons are being investigated.

1. Defects in the original substrate material which are transmitted and magnified in the grown layer.
2. Contamination of the initial substrate surface either due to chemisorbed impurities such as oxygen or due to dust particles. Contamination from the graphite heater may also occur during the growth run.
3. Too rapid a growth rate or a non-uniform growth rate. The latter condition may be present if the concentration of reactant gases or the temperature of the substrate is altered.

Though these structural growth faults have been observed and overcome in the epitaxial growth of silicon, germanium and gallium arsenide it should be realized that silicon carbide is different from these other materials because it may exist in two different structural forms, the cubic and the hexagonal structures. The latter structure has many polymorphic forms. The structure of the cubic form can be viewed as the stacking of tetrahedral sheets perpendicular to the trigonal axis of the cube, all sheets being equivalent. The structure of the various hexagonal

polymorphs can then be derived from the cubic form by rotating the sheets of tetrahedra in the proper layers so that they lie in parallel or anti-parallel orientation.

Since there are only slight differences in the structural free energies[9] and internal energies of these various forms of silicon carbide it is possible that slight changes in the growth conditions of temperature and concentration of gaseous reactants will produce structural defects.

2.4 APPLICATION OF EPITAXIAL GROWTH TO TRANSISTOR FABRICATION

It is anticipated that the epitaxial growth process will allow the growth of high purity thin layers of controllable thickness. Such layers would be very suitable for either the p base region of an npn drift transistor or an n type channel in a unipolar transistor.

Some preliminary experiments have been carried out on the growth of n type layers on p type substrates in order to evaluate the properties of the junction between the epitaxial layer and the substrate. Though these experimental results were preliminary and were not conclusive, evidence of rectification was obtained. This work will be continued since it is essential to produce a good junction between the grown layer and the substrate before a more elaborate structure such as a transistor may be fabricated.

3. DIFFUSION

Although the primary interest of this program is the preparation of a transistor (field effect) using epitaxial growth methods, a diffusion process is also being studied that may be used as a supplement to the epitaxial growth technique.

Two of the major difficulties in the fabrication of a silicon carbide transistor are the low mobility and the short lifetime of the minority carriers. The mobilities for electrons and holes in silicon carbide have been determined at 180 and 12 cm^2/volt. sec. respectively, while the lifetime for both holes and electrons is approximately 10^{-8} seconds (at 600°C). These material constraints require very close control of both the device structure and the impurity distribution in the junction region. Diffusion methods, where the process variables can be quite closely controlled, should be able to maintain the tolerances necessary for the device.

The diffusion technique was of the open system, flowing carrier gas type. A new furnace was designed and constructed for these experiments, utilizing the basic design shown in Figure 19, Final Report to Cambridge Research Laboratories, AF 19(604)-5997.[1] This new furnace incorporated many improvements designed to make the operation more reliable and to permit more extensive and detailed experiments. Some of these improvements are described below. A quartz tube serves both as an electrical insulator between the two electrodes to the graphite heater and as a vacuum and gas tight enclosure. The graphite heater is shaped so that the maximum temperature is at the center of the furnace. The ends of the heater are

pressed into conical contacts, one of the contacts being spring loaded to permit expansion of the graphite on heating. The quartz tube is shielded from the graphite heater by concentric cylinders of graphite and molybdenum. Since the diffusant vapors used will deposit on surfaces other than the sample crystals, the graphite heater must also be protected. To accomplish this a graphite sleeve is inserted inside the heater such that none of the diffusant vapors directly reach the heater. This sleeve is electrically insulated from the heater ends by glass tape.

The furnace temperature is sensed by a Leeds & Northrup Ray-O-Tube and controlled by a Leeds & Northrup DAT type controller-recorder. Recorder traces suggest variations of less than $\pm 1°C$ over an 18 hour diffusion run. However, other factors, such as fogging of the sight glass, permit a variation of at least $\pm$ 2°C. The temperature along the tube must be nearly constant for several inches if reproducible diffusion results (even within a single run) are to be obtained. A temperature mapping of the furnace indicates that the variation is no more than $\pm$ 1-1/2°C over a two inch length. There is also a small radial temperature gradient, but this is less important since the sample crystals are kept very near to the center line of the furnace.

The samples are placed on a graphite slab in a small closed graphite container. This is then placed in a second graphite cylinder that fits snugly into the protecting sleeve. Care must be taken to provide an equilibrium atmosphere of the Si-C-SiC reaction around the crystals. If this equilibrium is not maintained, the surfaces of the crystal will decompose (experimentally determined to be as high as 0.1 mil/hr) and there will be no stable surface for the diffusion reaction.

The diffusant (carefully weighed) is placed in a boron nitride boat which is fitted into a graphite holder. A rod, passing through an "O" ring seal is attached to this holder so that the diffusant material can be moved along the sleeve to a position of proper temperature.

The carrier gas used is a 95% argon - 5% hydrogen mixture. The flow rate can be controlled over a large range but thus far most of the work has been done with flow rates of about 300cc/min.

The diffusion process will be used to diffuse donors or acceptors onto a p or n type epitaxially grown substrates. Until these substrates are available diffusion runs are being made on silicon carbide crystals produced by the sublimation method using a Kroll-type furnace. These crystals are mainly n-type (nitrogen impurity) and vary in impority concentration from 10^{17} carriers/cc (determined by a light green hue) to less than 10^{16} carriers/cc (colorless). It is from runs on these crystals that the various experimental parameters are being investigated and optimized so that when epitaxially grown substrates are available, device preparation can proceed without undue delay. At present aluminum is being used as the diffusant although other donor or acceptor materials will be investigated.

As stated earlier the junction structure is of prime importance in producing a workable SiC transistor. It has been shown that the junction of a unipolar transistor must be abrupt as well as showing low leakage current with a high breakdown voltage. To produce these abrupt junctions parameters such as diffusing time and temperature, the different vapor concentration (infinite source vs limited source) and gas flow will be studied.

4. DEVICE TECHNIQUES

In the period before suitable epitaxially grown material is available, the device work has been directed toward perfecting our basic techniques as much as possible. The results are discussed under separate headings below.

4.1 ALLOYING CONTACTS

A new alloying furnace has been designed and built. This furnace uses a graphite heater to produce the high temperatures needed for alloying to silicon carbide. The design principle is essentially the same as reported previously[2] but the new design is vacuum-tight and precisely made. The furnace is more versatile in that it can be used with either a gaseous ambient or a high vacuum.

A great variety of materials may be applicable for contacting to silicon carbide. Tungsten is the best known contact material for silicon carbide mainly because its coefficient of thermal expansion matches the silicon carbide very closely, thereby introducing little strain in the contact region. However, the temperature required for alloying tungsten directly to silicon carbide is as high as 2000°C and the wetting is poor. At this high temperature the quality of the crystal may be deteriorated. Both tungsten and silicon carbide are hard and brittle, even a very small difference of their thermal expansions can introduce strains in the crystal. A logical approach in solving this problem is the use of a soft material for soldering the tungsten to silicon carbide at a lower temperature than 2000°C. This soft material should have good wetting to both silicon carbide and tungsten.

Several alloys have been investigated, such as silicon, platinum and their alloys[1,2]. The wetting of these alloys to silicon carbide is not very satisfactory. The alloying temperature is still too high ($> 1400°C$) and the alloys are not soft enough.

Based on the experience with the alloyed contacts to silicon, gold should be an ideal material for soldering because of its softness, low melting point (1063°C), and chemical inertness to most etches. It has been found, however, that the wetting of pure gold to silicon carbide is very poor.

One possible reason for poor wetting is the existence of an oxide layer or carbon atoms on the surface of silicon carbide. If that is the case, elements with a strong affinity for oxygen and carbon, added to gold, should improve the wetting. These elements should have very low diffusivities in silicon carbide, should not form eutectics with gold lower than about 1000°C, and should maintain the softness of gold. It appears that tantalum satisfies all these requirements.

The experimental work was started in this laboratory for the fabrication of power rectifiers. Gold containing small percentages ($\sim 1\%$) of tantalum and dopant can be alloyed onto silicon carbide to form low resistance contacts at temperatures of 1100°-1200°C. Metallurgical studies indicate that the wetting and penetration is very uniform, without any voids at the interface of the alloy and silicon carbide.

In order to apply the gold-tantalum alloy to the fabrication of silicon carbide transistor devices, the depth of penetration should be

accurately controlled. The new furnace will be used for the study of the depth of alloying as it relates to temperature and alloying composition.

4.2 ELECTROLYTIC ETCHING

Much of our effort has been expended improving our methods in this field. The results that have been achieved are not entirely conclusive. To obtain an accurate reproduction of etching, lateral etching must be minimized. It appears that the etching of restricted area may be greatly improved by using the conditions employed in electropolishing, i.e., very high current densities and viscous solutions. A solution of 15 cm^3 glycerine, 10 cm^3 nitric acid, and 6 cm^3 hydrofluoric acid was tried. A crystal was masked and a line 80μ wide was scribed. After electrolytic etching this scribed line was 122μ wide and 80μ deep with a lateral etching to vertical etching ratio of 0.35:1. A similar specimen was etched in a solution of the same acids except that acetic acid used in place of the glycerine. This sample showed a ratio of lateral etching to vertical etching of 5.4/1. Thus the lateral etching for the viscous solution was less than 1/15 of that of the non-viscous solution.

Another interesting result to come from these studies is the achievement of electrolytic etching of n-type silicon carbide using a forward-biased p-n junction as the source of holes. In one example of such of such etching a groove 5μ deep was etched in the n-face of a silicon carbide crystal in 2 minutes with the holes for etching being injected by a p-n junction. The distance separating the etched n-surface and the injecting junction was about 42μ.

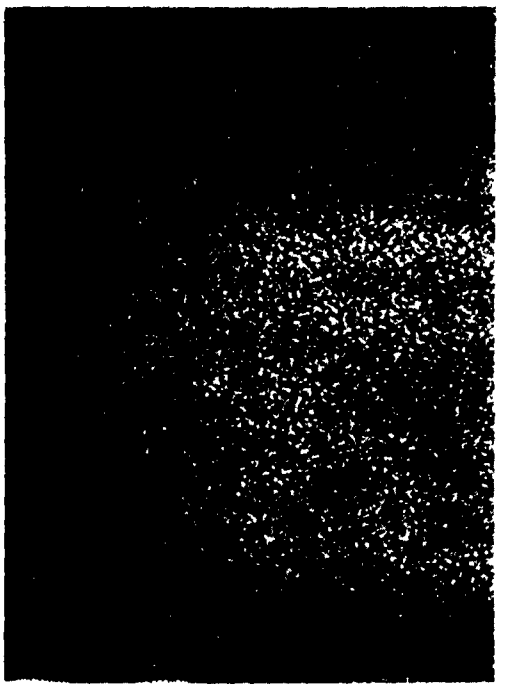
4.3 MOLTEN SALT ETCHING

Early in the present work a difficulty in using molten Na_2O_2 as an etch was noted. Due to its viscosity it was hard to pour, and it was difficult to extract the crystal from the solidified salt. To improve fluidity the addition of NaOH was tried, and a resulting improvement in the surface characteristics of crystals etched in these melts was noted. A series of etching experiments were made to determine the degree of improvement that could be expected from such melts. The melts had the following compositions: pure Na_2O_2; 3 Na_2O_2-1 NaOH; 1 Na_2O_2- 1 NaOH; 1 Na_2O_2- 3 NaOH; and pure NaOH. Lapped crystals were etched two minutes at 700°C in each of the melts. An examination of the crystals after etching showed that, as long as Na_2O_2 was present, the attack on the crystal was preferential, becoming less preferential as the concentration of NaOH in the melt was increased. Etch rates were determined for pure Na_2O_2 and the 1 Na_2O_2-3 NaOH mixture at 700°, both being 7μ per minute. The pure NaOH apparently attacks silicon carbide very slowly at this temperature.

The mixture of 1 Na_2O_2 - 3 NaOH gives surfaces on silicon carbide that are quite similar to those obtained by the CP4 etching of Ge or Si. A comparison between the surfaces obtained from etching in pure molten Na_2O_2 and those of the 1 Na_2O_2 - 3 NaOH mixture made may be obtained from Figures 4.1 (a,b) and 4.2 (a,b). In each case the (a) surface is the "good" side of the crystal and (b) side is the "bad" side of the crystal.

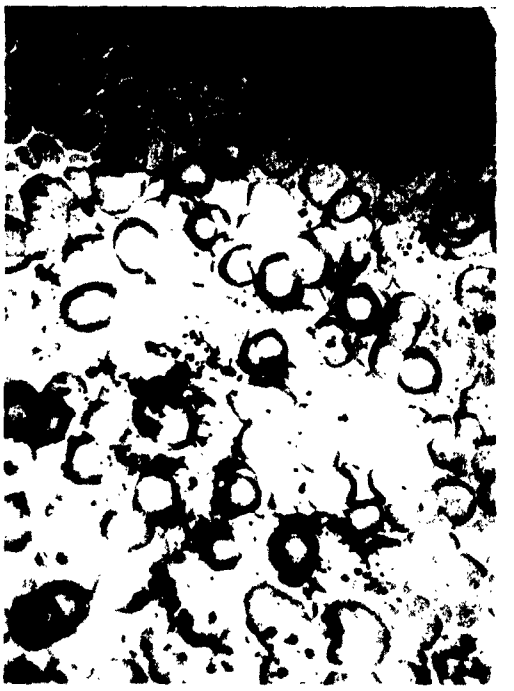
4.4 JUNCTION DELINEATION

The most satisfactory method yet devised for delineating p-n junctions in silicon carbide is the electrolytic etching of the p-region of



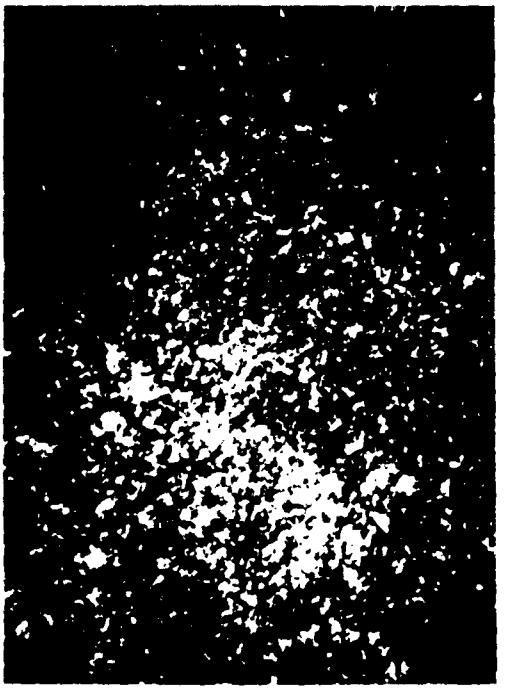
4.1 a [x 212]

SiC Crystal Etched in Na_2O_2
Good Side



4.2 a [x 212]

SiC Crystal Etched in 1
Na_2O_3-3 NaOH



4.1 b [x 212]

SiC Crystal Etched in Na_2O_2
Bad ("Wormy") Side

4.2 b [x 212]

SiC Crystal Etched in 1
Na_2O_2-3 NaOH
Bad ("Wormy") Side

the crystal by immersion in a solution of 100 methyl alcohol to 1 HF (MeOH-HF) under simultaneous forward or reverse bias. This method is not completely satisfactory and other methods have been tried. Figure 4.3 shows the result of one such trial. In this instance the n-side of the crystal was delineated by electroless nickel plating, which is the method used for obtaining electrical contact to the specimens. The electroless nickel bath is composed of 30 gms/l of hydrated nickel chloride; 10 gms/l of sodium hypophosphite, 65 gms/l of ammonium or sodium citrate and 50 gms/l of ammonium chloride. A small amount of ammonia is added to the bath to bring the pH to 7.0. The excellent delineation of the junction is shown in the figure. It is unfortunate that this method has provde to be less reproducible than MeOH-HF etching.

For comparison, a good example of MeOH-HF etching is shown in Figures 4.4 & 4.5. The edge of the crystal shown here was lapped on one side while the other side was cleaved. It was etched first under reverse bias (Figure 4.4) and then under forward bias (Figure 4.5), the p-side of the crystal being on the bottom in each case. An interesting phenomenon may be seen in the figures. Under reverse bias the edge of the etched region forms a continuous line across the boundary between the lapped and cleaved sides; under forward bias, however, the edge of the etched region does not form a continuous line across that boundary. On both the lapped side and the cleaved side the etched region is wider than that obtained under reverse bias, but the increase in width is greater on the cleaved side and exhibits itself as a second line lying above that obtained under reverse bias. If one looks closely at Figure 4.4 the edge of the etched

Fig. 4.3 [x 56]

Junction in SiC Delineated by Electroless Nickel Plating

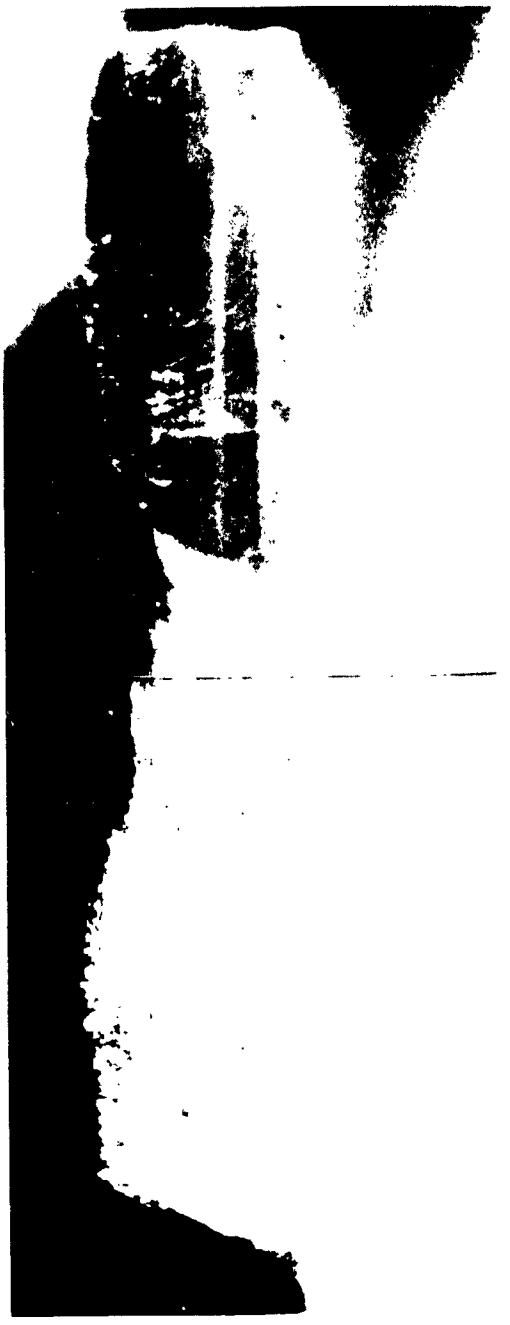


Fig. 4.4 [x 61]

SiC Crystal Etched in 100 Methyl Alcohol —
1 Hydrofluoric Acid Under Forward Bias

Fig. 4.5 [x 61]

SiC Crystal Etched in 100 Methyl Alcohol —
1 Hydrofluoric Acid Under
Reverse Bias

region on the lapped side appears to meet the cleaved region, at a point part way between the two lines obtained by forward and reverse bias. This is even more obvious when seen under the microscope. It would seem that the explanation of this phenomenon is that under reverse bias holes are extracted from a region near the junction having the same width on both sides of the junction. Under forward bias, however, the lapped surface acts as a sink for minority carriers so that the holes are recombined before any etching can occur; conversely, the cleaved surface allows etching to occur to approximately a diffusion length from the junction. Estimating the diffusion length from this phenomenon indicates that it is about 8μ at room temperature, a result that is in at least qualitative agreement with the hole-injection etching of n-type silicon carbide discussed previously.

4.5 MASKING

Etching accurately defined areas is essential in producing devices of controlled characteristics. The most successful approach to date has been to apply Fisher Pyseal, a waxlike cement, to the surface of the specimen and remove it in the prescribed areas by scribing. A constant-pressure, micromanipulator-mounted scribe has been built and is being used for this purpose. The results are promising as may be seen from the deep groove etching reported under 4.2 Electrolytic Etching above. The use of Kodak Metal Etch Resist for this purpose is being investigated, but the results are not yet conclusive.

5. UNIPOLAR TRANSISTOR

5.1 DEVICE ANALYSES

In material of low mobility and short lifetimes, such as

silicon carbide, the operation principle of the device should be based on the field effect rather than on carrier diffusion. The analyses have been made on two basic high frequency field effect devices — the n-p-n drift and unipolar transistors,[2] using the recent values of alpha-silicon carbide physical constants as listed in Table 1. The construction of the unipolar transistor for 1 mc operation is more feasible. For completeness, this qualitative analysis is included here.

TABLE I

PHYSICAL CONSTANTS OF ALPHA-SILICON CARBIDE AT 650 C

Band Gap	Eg	2.66 ev
Dielectric constant	K	9×10^{-13} Fcm^{-1}
Intrinsic carrier conc.	Ni	3.75×10^{12} cm^{-3}
Mobilities	μn	180 cm^{2}v^{-1} sec.$^{-1}$
	μp	12 "
Lifetime	n	10^{-8} sec.
	p	10^{-8} sec.
Diffusion Constant	Dn	14 cm^2 sec^{-1}
	Dp	1 "
Diffusion Lengths	Ln	3.9×10^{-4} cm.
	Lp	1.0×10^{-4} cm.
Effective mass	Mn	0.6 m_e
		1.2 m_e

The purest alpha-silicon carbide single crystal platelets prepared by Westinghouse are n-type with a donor concentration of 10^{14} - 10^{16} cm^{-3}. This purity corresponds approximately to a room temperature resistivity of 50 - 100 ohm-cm depending on the values of the electron mobility and carrier concentration.

The channel thickness 2a, is limited by the pinch-off voltage and the purity of silicon carbide, according to the equation[10]

$$a = (2KW_o/qN)^{1/2}$$

$$\cong 3.35 \times 10^3 (W_o/N)^{1/2} \text{ cm} \qquad (1)$$

where K is the dielectric constant, q the electron charge, W_o (volts) the pinch-off voltage, and $N(cm^{-3})$ the net ionic impurity concentration in the depletion region. According to Equation (1) the purity of the present material ($N = 10^{14}$ -10^{16} cm^{-3}) should give a half-channel thickness, a, in the range of 2 to 20 microns at which the pinch-off condition can occur at voltages as low as 25 volts. This half-channel thickness is well within the precision which the present diffused junction depth can be controlled. The vapor phase epitaxial growth technique will be more suitable for the formation of this junction structure.

Another limitation in the design of unipolar transistors is the allowable power dissipation in the unit. As suggested by Dacey and Ross,[11] a reasonable design criterion would be the power dissipated per unit area of channel, since the majority of the heat generated is conducted away through this area. This power per unit area P ($watt/cm^2$) can be expressed as

$$P = \frac{2}{3} W_o^2 (a/L)^2 / a\rho \qquad (2)$$

where L (cm) is the length of the channel and ρ (ohm-cm) the resistivity of the channel material. The power dissipation for a germanium unipolar transistor is about 400 watts per cm^2. Silicon carbide devices can be operated at more than 150°C above an ambient of 500°C, whereas germanium devices have a maximum operating temperature of about 50°C above room temperature. It appears reasonable to assume P = 1200 watts/cm^2 for the silicon carbide devices.

Suppose that the material has a net donor concentration of 5×10^{14} cm^{-3}. This purity corresponds to a resistivity of about 35 ohm-cm at 500°C. According to Equation (1), this material should give a half-channel thickness of about 7.5 microns at W_o = 24 volts. Then, for p = 1200 watts/cm^2, Equation (2) gives $\frac{a}{L} = 7.6 \times 10^{-2}$ and $L = 1 \times 10^{-2}$ cm or about 4 mils.

The remaining parameters, Z(cm), the width of the channel, determines the maximum channel current and the power dissipation. The maximum saturation current, J_{DO} (amperes), flowing through the channel when zero bias ($V_G = 0$) is applied to the gate can be expressed as

$$J_{DO} = \frac{2}{3} \frac{W_o Z}{\rho} (a/L) \qquad (3)$$

Suppose that Z = 1 mm. Then, from Equations (2) and (3), J_{DO} = 3.6 ma, and the power dissipation is about 4 watts.

The limiting frequency, f (cycles per sec), can be expressed as

$$f = \frac{1}{4\pi K \rho} \left(\frac{a}{L}\right)^2 , \qquad (4)$$

indicating that this transistor can be operated at a maximum frequency of about 15 mc.

5.2 FABRICATION STUDIES

One of the active devices to be fabricated under this contract is the unipolar field-effect transistor capable of one megacycle operation at 500°C having epitaxially grown junctions. Since good epitaxial silicon carbide is not yet available, attempts are under way to fabricate unipolar transistors from grown-junction and diffused materials.

The approach being used for the grown-junction transistor is shown in Figure 4.6. The crystals initially have an internal p-region surrounded by a double n-region, the n-material closest to the junction being nearly intrinsic and that farther away from the junction having a lower resistivity. In the fabrication of the device the edges of the crystal and the poorer of the junctions are removed by lapping, which exposes the central p-region on one face. Areas of the p-region, leaving a central portion of the p-region to act as one half of the gate. On the bottom side opposite the gate contact already formed, a region, to become the other half of the gate, is formed by etching the lower resistivity n-region away to allow a rectifying contact to be made to the high resistivity n-region. The latter etching is done using the hole-injection etching discussed earlier. The device is completed by applying suitable contacts to the various regions as shown in Figure 4.7.

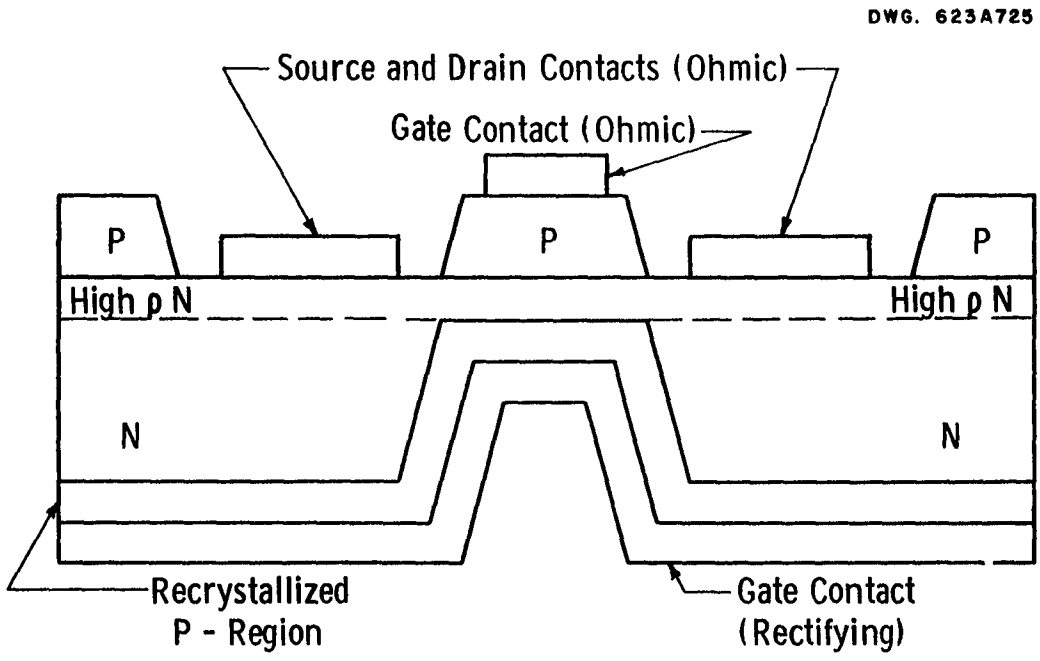


Fig. 4.6—Grown junction transistor

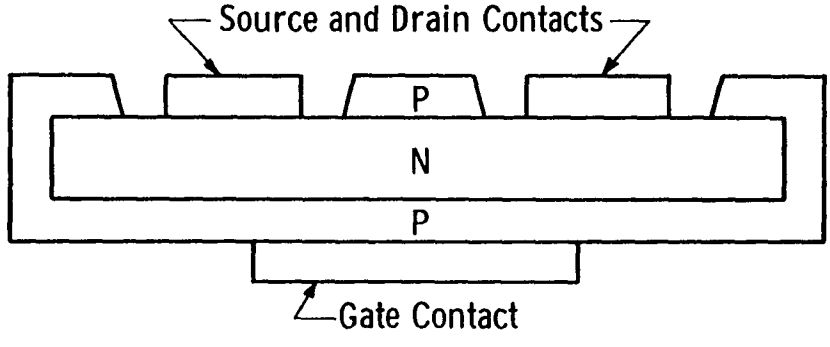


Fig. 4.7—Diffused junction transistor

The diffused junction unipolar transistor is shown schematically in Figure 4.7. In the fabrication of this device a high resistivity n-type crystal is diffused with aluminum to a depth sufficient to leave a thin n-region in the center of the crystal to act as the channel. Two areas are etched away, revealing the central n-region but leaving a strip of p-material between these areas to act as the gate. Ohmic contacts to the two exposed n-area and to the bottom of the crystal complete the fabrication.

6. SUMMARY AND CONCLUSIONS

The process of epitaxial growth has proved to be feasible. Grown layers have been formed and conditions for optimum growth are being determined. Further work is necessary to improve the perfection of the grown layer. Certain changes in the apparatus are also necessary so that the purity can be more closely controlled, and dopants introduced when desired. The fabrication of a device from an epitaxially grown junction crystal appears to be possible using techniques already developed.

The new diffusion furnace has performed quite satisfactorily. With the improvements earlier discussed better control of the experimental variables is obtainable. In order to control the depth of diffusant penetration and the junction gradient more exactly, a two step diffusion process will be investigated. In this method a high concentration of the impurity is diffused onto the crystal surface in a short time, and diffusion into the crystal proceeds without further diffusant being added to the system.

Concurrently a detailed investigation of the energy levels of various donors and acceptors in silicon carbide should be planned. This data should indicate methods for increasing the temperature range of usability for a silicon carbide device as well as permitting greater latitude in device fabrication techniques.

The penetration of the alloyed contact must be closely controlled. The depth and the electrical properties of the contact as a function of chemical composition and alloying temperature should be studied.

The fundamental methods for device fabrication have now been established. Work on device fabrication will be performed on crystals containing diffused junctions. When the epitaxially grown junctions are available the emphasis will be shifted to these crystals.

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PREVIOUS AND RELATED CONTRACTS

1. Air Force Cambridge Research Center — AF 19(604)-2174
   Research in the Preparation of Hyperpure Single Crystal Silicon Carbide
2. Wright Air Development Center — AF 33(600)-34953
   Power Rectifier Development Program
3. Air Force Cambridge Research Center — AF 33(616)-5592
   Research on Silicon Carbide Transistors
4. Air Force Cambridge Research Center — AF 19(604)-5997
   Study, Development, and Application of Techniques Necessary to Fabricate Active Silicon Carbide Devices
5. Aeronautical Systems Division — AF 33(657)-7027
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